A THICK OXIDE P-GATE NMOS CAPACITOR FOR USE IN A PHASE -LOCKED LOOP CIRCUIT AND METHOD OF MAKING SAME

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to semiconductor devices and, in particular, to a thick oxide P-gate NMOS capacitor for use in a phase-locked loop circuit and methods for making the same.

Background Art

[0002] A phase-locked loop (PLL) synthesizer circuit is a negative feedback circuit that operates so as to bring a set frequency into conformity with an output signal frequency. PLL synthesizer circuits are used for automobile telephones, portable telephones, radios, televisions, cable modem tuners, and the like. As circuit integration and the desire for faster circuits increase, circuit designers are faced with new challenges to implement known functionality, such as in ability to maintain lock in a PLL synthesizer circuit.

[0003] An example of a conventional PLL synthesizer circuit will be explained with reference to FIGS. 1-3 of the accompanying drawings. A quartz oscillator 102 outputs a reference clock signal "CK" of a natural frequency based on the oscillation of a quartz oscillation element to a reference frequency divider 104. The reference frequency divider 104 divides the frequency of the reference clock signal CK on the basis of a set frequency, which is externally set, predetermined, or is otherwise programmed, and outputs a reference signal "fr" to a phase comparator 106. A comparison frequency divider 108 outputs a comparison signal "fp" to the phase comparator 106. The phase comparator 106 compares the

reference signal fr with the comparison signal fp, and outputs pulse signals "φR" and "φP", which correspond to the frequency difference and phase difference, respectively, to a charge pump 110.

[0004] The charge pump 110 outputs a signal "SCP" (charge pump signal) on the basis of the pulse signals φR, φP output from the phase comparator 110, to a low-pass filter (hereinafter referred to as "LPF") 112. This output signal SCP contains a pulse component in its D.C. component. The D.C. component rises and falls with the frequency changes of the pulse signals φR, φP, while the pulse component changes on the basis of the phase difference of the pulse signals φR, φP.

[0005] The LPF 112 smooths the output signal SCP of the charge pump 110, and outputs a signal "SLPF" (LPF signal), from which a radio frequency (RF) component is removed, to a voltage controlled oscillator (hereinafter referred to as "VCO") 114. The VCO 114 outputs a signal "SVCO" (VCO signal) having a frequency corresponding to the voltage value of the output signal SLPF of the LPF 112 to an outside circuit (not shown) and to the comparison frequency divider 108 described above. The comparison frequency divider 108 divides the frequency of the output signal SVCO of the VCO 114 by a necessary factor and outputs it to the phase comparator 106.

[0006] As shown in FIG. 2, an unlock condition results when a setting of the comparison signal fp, for example, is changed such that the frequency and/or phase of the reference signal fr are not in conformity with those of the comparison signal fp. When these differences in the frequencies and phases of the reference signal fr and the comparison signal fp occur, the phase comparator 106 outputs the pulse signals φR and φP. The D.C. component of the output signal SCP of the charge pump 110 is passed by LPF 112. The voltage level of

the output signal SLPF of the LPF 112 rises on the basis of the output signal SCP, and the output signal SLPF of the LPF 112 converges to a voltage level corresponding to the comparison signal fp set afresh, and the operation mode returns to the lock state.

[0007] When the frequency of the comparison signal fp of the PLL synthesizer circuit is lowered as described above, the output signal SLPF of the LPF 112 rises from V1 to V2 as indicated by a solid line in FIG. 3, for example. However, since the phase difference occurs even when the frequency of the reference signal fr is in conformity with that of the comparison signal fp, the output signal SLPF, which has risen to a point near V2, converges with V2 while repeating an over-shoot and under-shoot.

[0008] Prior art integrated versions of the PLL of FIG. 1 typically implement the LPF 112 using a simple RC circuit. The capacitor of the RC circuit has comprised a PMOS FET (P-type metal oxide semiconductor field effect transistor). FIG. 4 is a schematic diagram of a PMOS FET configured as a capacitor. The capacitance is formed by the gate capacitance and the depletion capacitance in series. If the transistor is in the strong inversion mode ($V_{GS} > V_{TH}$), the gate capacitance is the sole contributor of the total capacitance.

[0009] The gate capacitance is inversely proportional to the thickness of the gate oxide. As the technology advances, the thickness of the gate oxide of the transistor decreases, thus increasing the capacitance. However, a decrease of the gate oxide thickness causes the leakage current through the agate to increase. In the LPF 112 of the PLL circuit in FIG. 1, the gate voltage across the capacitor is used to control the VCO 114, which outputs the desired frequency SVCO. If there is gate leakage in the PMOS FET capacitor the control voltage will not be held constant and will cause drift in the output frequency of VCO 114.

[0010] What is needed is a technique to obtain stable a PLL control voltage, without drastically increasing the complexity and cost of the circuit.

BRIEF SUMMARY OF THE INVENTION

[0011] The present invention is directed to a phase locked loop circuit. The circuit includes an oscillator to output a reference clock signal; a reference frequency divider to receive and divide the reference clock signal, and output a reference signal; a comparison frequency divider to receive a control voltage and output a comparison signal; a phase comparator to receive the reference signal and the comparison signal, wherein the phase comparator compares the reference signal with the comparison signal and outputs a frequency difference signal and a phase difference signal; a charge pump to receive the frequency difference and the phase difference signals and output a charge pump signal; a low-pass filter to receive the charge pump signal and output a low pass filter signal; and a voltage controlled oscillator to receive the low pass filter signal and output the control voltage signal. The low-pass filter comprises a capacitor formed by an N-type substrate, a P-type region formed on the N-type substrate, a thick oxide formed over the P-type region, a P^+ gate electrode formed over the thick oxide and coupled to a first voltage supply line, and P^+ pick-up terminals formed in the P-type region adjacent the gate electrode and coupled to a second voltage supply line.

[0012] In another embodiment the present invention, a low-pass filter for a phase locked loop (PLL) circuit includes a capacitor, comprising: an N-type substrate, a P-type region formed on the N-type substrate, a thick oxide formed over the P-type region, a P^+ gate electrode formed over the thick oxide and coupled to a first

voltage supply line, and P^+ pick-up terminals formed in the P-type region adjacent the gate electrode and coupled to a second voltage supply line. A gate-to-substrate voltage is maintained at less than zero volts to maintain a stable control voltage for the PLL.

[0013] In yet another embodiment according to the present invention, a semiconductor device, functioning as a capacitor, comprises an N-type substrate, a P-type region formed on the N-type substrate, a thick oxide formed over the P-type region, a P^+ gate electrode formed over the thick oxide and coupled to a first voltage supply line, and P^+ pick-up terminals formed in the P-type region adjacent the gate electrode and coupled to a second voltage supply line.

[0014] These and other advantages and features will become readily apparent in view of the following detailed description of the invention.

BRIEF DESCRIPTION OF THE FIGURES

[0015] The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit of a reference number identifies the drawing in which the reference number first appears.

[0016] FIG. 1 illustrates a conventional PLL circuit.

[0017] FIGS. 2 and 3 are plots of signals corresponding to the circuit of FIG. 1.

[0018] FIG. 4 is a schematic diagram of a PMOS FET configured as a capacitor.

[0019] FIG. 5 illustrates the structure of a P-gate NMOS semiconductor device 500, according to an embodiment of the present invention.

[0020] FIG. 6 is a plot of capacitance verses voltage (C-V) for a P-gate NMOS capacitor, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0021] The preferred embodiment of the present invention will now be discussed in detail. While specific features, configurations and arrangements are discussed, it should be understood that this is done for illustration purposes only. A person skilled in the relevant art will recognize that other steps, configurations and arrangements or devices may be used to achieve the features of the invention without departing from the spirit and scope thereof. Indeed, for the sake of brevity, conventional electronics, manufacturing of semiconductor devices, and other functional aspects of the method/apparatus (and components of the individual operating components of the apparatus) may not be described in detail herein.

[0022] The terms, chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

[0023] Historically, the material most commonly used in the semiconductor industry to form the gate insulator layer of a field effect transistor (FET) is silicon

dioxide. Thus the gate insulator layer is frequently referred to simply as the gate oxide. The expression gate dielectric is also used to describe the gate insulator layer.

[0024] The term "gate" is context sensitive and can be used in two ways when describing integrated circuits. Gate refers to a circuit for realizing an arbitrary logical function when used in the context of a logic gate. However, as used herein, gate refers to the insulated gate terminal of a three terminal FET when used in the context of transistor circuit configurations or formation of transistor structures. The expression "gate terminal" is generally interchangeable with the expression "gate electrode". A FET can be viewed as a four terminal device when the semiconductor body is considered, for the purpose of describing illustrative embodiments of the present invention, the FET will be described using the traditional gate-drain-source, three terminal model.

[0025] Polycrystalline silicon is a nonporous form of silicon made up of randomly oriented crystallites or domains. Polycrystalline silicon is often formed by chemical vapor deposition from a silicon source gas or other methods and has a structure that contains large-angle grain boundaries, twin boundaries, or both. Polycrystalline silicon is often referred to in this field as polysilicon, or sometimes more simply as poly. Polysilicon is commonly used as the gate terminal of FET devices.

[0026] Source/drain terminals refer to the terminals of a FET, between which conduction occurs under the influence of an electric field, subsequent to the inversion of the semiconductor surface under the influence of a vertical electric field resulting from a voltage applied to the gate terminal. Generally, the source and drain terminals are fabricated such that they are geometrically symmetrical. With geometrically symmetrical source and drain terminals it is common to

simply refer to these terminals as source/drain terminals, and this nomenclature is used herein. Designers often designate a particular source/drain terminal to be a "source" or a "drain" on the basis of the voltage to be applied to that terminal when the FET is operated in a circuit. However, as described below, since the semiconductor device described herein does not function as a transistor in the conventional sense, the geometrically symmetrical regions that provide a supply voltage are called "pick-ups" rather than source and drain.

[0027] In conventional integrated circuit processing, FETs are fabricated with a single gate dielectric thickness. Although there may be some slight variation in gate dielectric thickness across a wafer, typically the result of manufacturing anomalies, these differences in dielectric thickness are usually too small to make any substantial difference in the electrical characteristics of the FETs of an integrated circuit, particularly with respect to the ability of those FETs to withstand a higher operating voltage. More recently, processing techniques permit FETs more than one gate dielectric thickness. Thus, on the same chip, designers can select to fabricate some FETs with a first gate dielectric thickness and other FETs with a second gate dielectric thickness.

[0028] As discussed below, the following more fully describes the present invention.

[0029] In 0.13μm (micron) technology, the inventors have observed that although increasing the thickness of the gate oxide of the PMOS FET capacitor in the LPF of the PLL circuit solves the basic leakage problem, another problem can arise. In addition to the reduction in gate oxide thickness, technology advances cause reduction in the supply voltage necessary to operate the smaller devices. Thus, the threshold voltage of the transistor having a thicker gate oxide is approximately equal to 0.6 V (volts), as compared to 0.3V in the thin oxide

0.13μm-technology transistors. In the PLL application described above, the control voltage can vary from 0.2V above ground to 0.3V below the supply voltage (V_{DD}). (Those skilled in the art would appreciate that the selection of the voltage level for the voltage supply typically depends on the type of fabrication technology used to manufacture the circuitry.) As a result, a transistor with a thick gate oxide may not be able to turn on depending on the control voltage level. The above voltage values are process-dependent and provided by way of examples only, and not limitation.

[0030] To solve this problem the inventors developed a P-type doped gate ("P-gate") NMOS device. An exemplary structure of a P-gate NMOS semiconductor device 500 according to the present invention is illustrated in FIG. 5. Semiconductor device 500 comprises a P-type region or substrate 504 formed in a N-type substrate 506. (As would become apparent to a person skilled in the relevant art, the conventions "P-type" and "N-type" represent nominal doping levels, as compared to higher doped regions commonly designated P^+ or N^+, or lightly doped regions commonly designated P^- or N^-.) Substrate 506 can comprise a deep N-type well ("NWELL"). In an alternative embodiment, the deep NWELL can be formed in or on another substrate.

[0031] A thick oxide 508 is formed on the region/substrate 504. The thick oxide 508 can comprise silicon dioxide, silicon nitride, or the like, as would be apparent to a person skilled in the semiconductor art. The thick oxide can be formed to a thickness of between about 20 and 100Å (Angstroms). The thick oxide material and specific thickness are application (e.g., depending on the applied voltage) and/or process (e.g., 0.13μm-technology) specific, as would become apparent to a person skilled in the releveant art.

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[0032] A polysilicon gate electrode 510 is doped with a P^+ dopant. Other gate structures will become apparent to persons skilled in the relevant art. P^+ doped pick-up terminals 512 and 514 are formed in the P-substrate 504.

[0033] To form a capacitor, region 504 of the device 500 is coupled to a first (e.g., positive $+V_{DD}$) voltage supply line +ve via the pick-up terminals 512 and 514, and the gate 510 is coupled to a second (e.g., negative or ground) voltage supply line -ve.

[0034] In this configuration, the device of FIG. 5 operates like an NMOS transistor in an accumulation mode with a shifted threshold voltage (V_{TH}). This $V_{TH\text{-}NEW}$ shift is shown at curve 602 in capacitance versus voltage (C-V) plot of FIG. 6. The magnitude of the shift is about 1V, compared to the nominal $V_{TH\text{-}OLD}$ of an NMOS transistor, represented by curve 604. According to the present invention, the device 500 can maintain operation in the accumulation mode when its gate-to-substrate voltage is less than zero volts. Region 606 represents the operational mode of device 500. As curve 602 implies, at region 606 device 500 maintains an operational capacitance C1. Area 608 represents the accumulation region of an NMOS transistor. Area 610 corresponds to an enlarged accumulation region of device 500.

[0035] The low pass filter 112 of FIG. 1 is used to filter out high frequency components of the SCP signal. According to an embodiment of the present invention, filter 112 can comprises a P-gate NMOS semiconductor device 500, as described above in connection with FIG. 5. The charge pump 110 preferably accumulates electrical charge based on the difference signals and provides a voltage control signal with sufficient current to the VCO 114 to adjust phase and/or frequency of the VCO output.

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94 **[0036]** The PLL is shown in FIG. 1 is for illustrative purposes only. The present invention can be applied to an PLL circuit, as well as any other circuit including a LPF.

[0037] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention as defined in the claim(s). Among other reasons, this is true in light of (later) developing technology and terms within the relevant art(s). Thus the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

[0038] For example, the present invention has been described with reference to a P-gate NMOS device formed in an NWELL. However, those skilled in the art would appreciate that P-type and N-type dopant types could be reversed to form an inverse device that would function very similar to the present invention given proper biasing modification that would also become apparent based on the above description.